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APPLICATION FOR LETTERS PATENT

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A METHOD TO FORM A CORRUGATED STRUCTURE FOR ENHANCED CAPACITANCE

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A METHOD TO FORM A CORRUGATED STRUCTURE FOR ENHANCED CAPACITANCE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of application Serial No. 09/651,946, filed August 31, 2000, pending.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates to a method of fabrication of a corrugated structure having enhanced capacitance characteristics. More specifically, the present invention relates to a method of forming a corrugated capacitor cell comprising multiple layers of alternating material having differing etch rates, hereby facilitating formation of rippled or corrugated capacitor walls for capacitor cells of semiconductor memory devices.

[0003] State of the Art: Dynamic random access memory, otherwise known as a DRAM memory chip, die, or device, is a popular type of semiconductor memory device. A DRAM memory device is essentially multiple arrays formed by a series of memory cells including a transistor, such as a metal oxide semiconductor field effect transistor (MOFSET) and an associated capacitor connected thereto fabricated on a substrate, such as a silicon substrate. The memory cells are combined with peripheral circuits to form the DRAM device. The state of the memory cell, either charged or uncharged, represents the state of a binary storage element, zero or one, (data) stored by the DRAM device in the memory cell. Multiple capacitors on a single silicon substrate or chip are therefore capable of storing large amounts of data. The greater the number of capacitors formed on a substrate or chip, the greater the memory capabilities of the DRAM memory device.

[0004] The popularity of the DRAM memory device is a direct result of the low cost involved in the production and manufacture of large quantities of DRAM memory devices. However, as the demand for smaller semiconductor substrates or chips with larger storage capacities has evolved, the ability to produce DRAM memory devices meeting the new technological requirements becomes increasingly difficult. This is particularly evident as the size of the capacitor cell becomes increasingly smaller. As the capacitor cell size of a DRAM memory device decreases in size, the area of the memory substrate or chip allocated for the

capacitor cell decreases in size, making it more difficult for the capacitor cell to store the required electrical charge for the desired period in the capacitor cell during operation of the DRAM memory device. It is necessary to address the demands for greater capacitor cell storage for DRAM memory devices which are ever decreasing in size.

[0005] One solution which is capable of providing the necessary number of capacitors on a DRAM memory device is the formation of stacked-type or trench-type capacitor cells having larger surface areas. Typical manners which may be used for increasing capacitor cell surface area for stacked-type capacitor cells are to use either fin-type capacitor cells, pillar-type capacitor cells, striated capacitor cell walls, rippled capacitor cell walls, or roughened-surface-type capacitor cell walls. Such types of stacked capacitor cells are described in United States Patents 5,061,650, 5,240,871, 5,300,801, 5,466,627, 5,519,238, 5,623,243, 5,637,523, 5,656,536, 5,827,783, 5,843,822, and 5,879,987. It is further known to selectively texturize polysilicon electrodes with respect to neighboring dielectric surfaces in DRAM memory devices, such as described in United States Patent 5,830,793.

[0006] However, construction of such capacitors having an increased surface area capacitor cell wall or electrode typically requires a restructuring of the process flow to facilitate manufacture of the capacitor cells. Further, the types of materials used for such capacitors having an increased surface area may require additional time for deposition or be difficult to deposit in a uniform manner using conventional deposition apparatus.

[0007] What is needed is a simple process for the construction of capacitor cells having increased wall area using existing equipment and processes so that existing process flow does not need to be altered or slowed down for the deposition process.

BRIEF SUMMARY OF THE INVENTION

[0008] The present invention comprises a method of forming a rippled or corrugated capacitor cell wall having increased surface area used in capacitors in DRAM memory chips and semiconductor devices. More specifically, the invention relates to a method of forming a rippled or corrugated capacitor cell wall having increased surface area in a DRAM memory device using alternating layers of silicate glass which are subsequently etched to form the corrugated cell wall structure. The corrugated capacitor cell is constructed of alternating layers of germanium boro-

phospho silicate glass (Ge-BPSG) and boro-phospho silicate glass (BPSG) or nitro silicate glass (NSG) and etched to form the rippled or corrugated cell wall. The formation of corrugated wall capacitor cells using the methods disclosed herein may be accomplished using current semiconductor device process technologies for materials having deposition rates comparable to those of the materials normally used for deposition in such process technologies.

[0009] Alternating layers of Ge-BPSG and BPSG, or NSG, are deposited on electrical contacts of a DRAM memory device or Metal Oxide Semiconductor Field Effect Transistor (MOSFET) using chemical vapor deposition (CVD) processes or plasma enhanced chemical vapor deposition processes (PECVD) using suitable apparatus operating at either atmospheric pressure levels or sub-atmospheric pressure levels. The layers are deposited in clusters such that individual capacitance cells are formed having trenches or spaces between each capacitance cell. Once the desired capacitance cell thickness is reached, the capacitance cells are capped with an etch-resistant layer. Introduction of either a wet or dry etchant into the trenches between the capacitance cells, however, etches the alternating layers at varying rates, thereby forming the rippled or corrugated wall of each capacitor cell. The form of the rippled or corrugated configuration of the capacitor cell wall is dependent upon the etch rates of the alternating layers, and specifically on the concentration of germanium (Ge) in the Ge-BPSG layers forming the capacitor cell.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

[0011] FIG. 1 illustrates a cross-sectional side view of a corrugated capacitor of the present invention;

[0012] FIG. 1A illustrates a cross-sectional side view of a corrugated capacitor of the present invention having a dielectric layer and a top electrode layer;

[0013] FIG. 2 illustrates a cross-sectional side view of the deposition of a first layer of doped silicate glass;

[0014] FIG. 3 illustrates a cross-sectional side view of the deposition of a first layer and a second layer of doped silicate glass;

[0015] FIG. 4 illustrates a top plan view of a semiconductor component having an array of capacitance units formed from the alternating first layers and second layers of doped silicate glass; and

[0016] FIG. 5 illustrates a cross-sectional side view of the formation of an etch-resistant layer over the alternating first layers and second layers of doped silicate glass prior to etching.

DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0017] Referring to drawing FIG. 1, the rippled or corrugated capacitor cell 100 of the present invention comprises a series of alternating first layers 110 and second layers 120 of doped silicon glass having rippled or corrugated sides, sandwiched between an electrical contact 140 located on a substrate 10 and an etch-resistant layer 130. The doped silicon glass of the first layer 110 and the doped silicon glass of the second layer 120 preferably have different etch rates such that etching contributes to the corrugated or rippled nature of the side wall surface 115 of each corrugated capacitor cell 100. Illustrated in drawing FIG. 1 is a representative construction for a corrugated side wall surface capacitor cell 100. If desired, a layer of material 111, such as silicon dioxide, may be applied over the initial first layer 110 of doped silicon glass before the deposition of a second layer 120 of doped silicon glass thereover to serve as an etch stop during the formation of the corrugated capacitor cell 100 by an initial etching process of alternating layers of first layers 110 of doped silicon glass and second layers 120 of doped silicon glass.

[0018] The corrugated capacitor cell 100 of drawing FIG. 1 is formed by a series of steps as illustrated in drawing FIGS. 2 through 5. Illustrated in drawing FIG. 2 is the deposition of a first layer 110 of doped silicon glass over an electrical contact 140 located on a MOSFET or similar semiconductor component on a silicon substrate 10. If such electrical contact 140 is not present on the semiconductor component to which the corrugated capacitor cell 100 is being formed, a suitable electrical contact 140 must first be deposited on the semiconductor component using methods as known in the art.

[0019] The first layer 110 of doped silicon glass is deposited over the electrical contact 140 by methods which provide a high deposition rate of formation. Such methods include CVD or PECVD. The first layer 110 of doped silicon glass is typically BPSG or NSG.

[0020] Deposition of a second layer 120 of doped silicon glass, typically Ge-BPSG, over the first layer 110 is illustrated in drawing FIG. 3. As with the first layer 110, the second layer 120 is deposited using CVD and PECVD techniques. Alternate layering of first layers 110 and second layers 120 forms a capacitor cell having a desired thickness. Deposition of the alternating layers occurs in a cluster formation, in either atmospheric or subatmospheric conditions in a reaction chamber known in the art. Deposition of the first layer 110 and second layer 120 thereby forms individual capacitance units which ultimately result in individual corrugated capacitor cells 100 of substrate10 as depicted in drawing FIG. 4.

[0021] As depicted in drawing FIG. 5, an etch-resistant layer 130 is deposited upon the uppermost surface of the last layer of doped silicon glass. The etch-resistant layer 130 inhibits degradation of the uppermost surface of the last layer of doped silicon glass during subsequent etching processes.

[0022] Compositions of BPSG, NSG, and Ge-BPSG lend themselves to both dry and wet etching. Application of dry or wet etching to the structure illustrated in drawing FIG. 5 produces the corrugated capacitor cell 100 depicted in drawing FIG. 1. The rippled or corrugated nature of the sides of the corrugated capacitor cell 100 result from the difference in etch rates between the first layers 110 and the second layers 120 of the corrugated capacitor cell 100. The etch rate of Ge-BPSG is different than the etch rate of BPSG. This holds true even when the concentrations of boron (B) and phosphorus (P) are the same in Ge-BPSG and BPSG. It has been found that by altering the concentration of germanium (Ge) in the Ge-BPSG, the etch rate of the Ge-BPSG may be modulated, thereby providing the ability to alter the corrugated nature of the sides of the corrugated capacitor cell 100 according to the concentration of Ge in the Ge-BPSG. The ability to modulate the etch rate of the Ge-BPSG layers of the corrugated capacitor cell 100 provides a convenient method by which corrugated capacitor cells 100 may be formed more readily over the methods of the prior art.

[0023] Formation of corrugated capacitor cells 100 on semiconductor structures, such as DRAM memory devices, by the described method is advantageous because the method

conforms with current processing techniques, thereby improving the throughput of memory chips due to higher deposition rates and faster etch rates of Ge-BPSG, BPSG, and NSG with the ability to use conventional process equipment.

[0024] Referring to drawing FIG. 1A, after the corrugated capacitor cells 100 are formed having corrugated or rippled side wall surface 115, a dielectric layer 116 is deposited over the side wall surface 115 and the upper etch-resistant layer 130. The dielectric material may be Si_3N_4, Ta_2O_5, BST, etc. After the dielectric layer 116 is deposited, an anneal process is performed on the substrate 10 used to form the semiconductor die for the redistribution of dopants used therein. Subsequently, a top electrode layer 118 is deposited over the dielectric layer 116 to form the top electrode for each capacitor cell 100. The material used for the layer 118 forming the top electrode of the capacitor cell 100 may be Si-Ge.

[0025] Having thus described certain preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof as hereinafter claimed.